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Electrically Controlling and Monitoring InP Nanowire Growth from Solution

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ABSTRACT Indium phosphide nanowires are of significant technological interest for applications ranging from single junction solar cells to high speed electronics. However, the efficient placement and integration of nanowires into devices remains a significant challenge. Here we extend the technique of electrically controlled solution—liquid—solid (EC-SLS) catalytic nanowire growth to indium phosphide. We are able to control the amount of nanowire growth by varying the bias voltage between the electrodes in solution, and to monitor nanowire bridging across the electrodes by recording the conductivity as a function of growth time. The as-grown indium phosphide nanowires exhibit n-type conductivity as was determined by the *in situ* integration of nanowires into a field effect transistor geometry. The ability to monitor nanowire growth and electrically control nanowire placement are valuable tools for fabricating nanowire devices. The EC-SLS process has the potential to aid in the fabrication of nanowire devices that could find applications in nanoelectronics, and as electrodes in solar cells and batteries.

KEYWORDS: indium phosphide · nanowire · bismuth · voltage · electric field · EC-SLS

Indium phosphide nanowires have been grown from catalyst particles using laser ablation,[1] metal organic chemical vapor deposition (MOCVD),[2−4] and the solution−liquid−solid (SLS) process.[5−11] In the SLS process,[5] precursors in solution are delivered to heated catalyst particles, which serve as seeds for nanowire growth. Solution phase synthesis is potentially more cost-effective than vapor phase techniques, because no expensive vacuum equipment is needed. In addition, the lower growth temperatures, typically below 300 °C,[12] make solution phase synthesis attractive for semiconductor processes not compatible with higher temperatures.

A recent report has demonstrated that CdSe nanowires can be controllably grown between two electrodes *via* the electrically controlled solution−liquid−solid (EC-SLS) method by varying the electrochemical potential of the catalyst seed particles.[13] The EC-SLS method enables the simultaneous synthesis and integration of nanowires into device geometries. In this article, we extend the EC-SLS technique to the growth of InP nanowires. An important new aspect is our ability to observe nanowire bridging, *in situ*, by measuring the conductivity across the biased electrodes during nanowire growth. In addition, we demonstrate the ability to directly integrate InP nanowires into devices by growing InP nanowires in a field effect transistor geometry. Structures fabricated using the EC-SLS scheme could be applied to nanoelectronics,[1,14,15] light emitting diodes,[16−18] solar cells,[19−24] and batteries.[25]

RESULTS AND DISCUSSION

A schematic of the experimental setup used to grow InP nanowires using the EC-SLS method is shown in Figure 1a. To make the substrate and mount resistant to the reaction conditions, only chemically inert and heat resistant materials such as glass, stainless steel, and Teflon were used. An optical image of a mounted sample can be seen in Figure 1b. The samples consisted of fused silica substrates with three pairs of interdigitated electrodes composed of a 5 nm titanium adhesion layer, a 75 nm platinum layer, and a 20 nm bismuth layer. The bismuth layer dewets and forms islands with diameters of roughly 50−100 nm, that serve as catalyst seed particles.[13,26] The channel length of each electrode pair was ~55 mm and the gap width was ~10 μm (see Figure 2a). During a reaction, the sample was immersed in a tri-*n*-octylphoshine (TOP) solvent at a temperature of 285 °C (see Figure 1a). Next, a bias voltage was applied and a precursor solution containing indium(III)−iodide and tris(diethyl amino) phosphine in oleyl amine was injected dropwise over the course of 3 min. After precursor injection, the samples were

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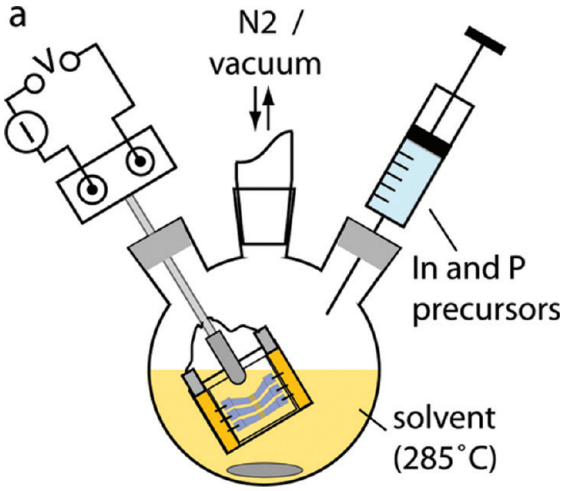


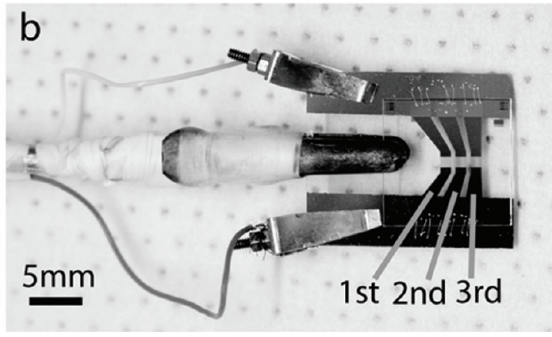
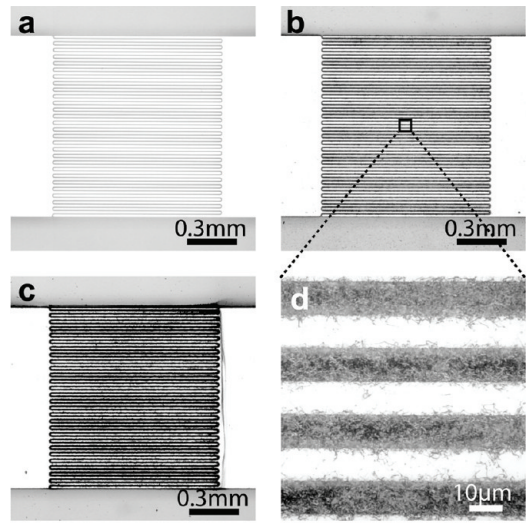


Figure 1. Experimental setup. (a) Schematic of the setup used to grow InP nanowires off Bi catalyst particles on Pt electrodes in solution. The temperature of the solution was monitored with a thermocouple inserted through a fourth neck (not shown). (b) Optical image of the sample holder; scale bar = 5 mm. Three interdigitated electrodes labeled 1st, 2nd, and 3rd can be biased in parallel, allowing for three separate devices to be fabricated simultaneously.



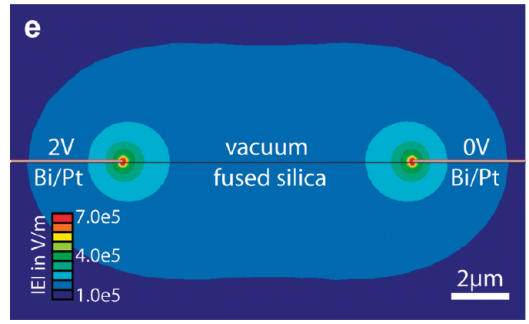


Figure 2. InP nanowire growth as a function of bias voltage. (a) Optical image of a pair of interdigitated electrodes without nanowires; (b) same geometry as in panel a after InP nanowire growth at a bias of 0.5 V; and (c) after growth at a bias of 2.0 V. The scale bars in panels a−c are 0.3 mm. (d) Highlighted region in panel b at higher magnification; scale bar = 10 μm. (e) Schematic of the cross-section of two adjacent electrode edges (to scale), including a simulation of the absolute magnitude of the electric field at a bias of 2 V; scale bar = 2 μm.

left in solution under constant temperature and bias voltage for another 2 min, before being withdrawn from the growth-solution.

Optical images of the interdigitated electrode geometry before and after growth at 0.5 and 2 V can be seen in Figure 2 panels a, b, and c, respectively. The nanowires are almost completely confined to the gaps between the electrodes, indicating that growth emanates from the electrode edges and is guided across the gap by the electric field. The correlation between electric field strength and, hence, surface charge density on the electrode and the focusing of nanowire growth along the electrode edges is supported by the simulation of the electric field strength in Figure 2e.[27] In particular, the well-known effect of electric field bunching at the edges of thin metal sheets is easily seen.[28] As in the case of CdSe,[13] InP nanowire growth is promoted on the low potential electrode (see also Supporting Information).

Characterization of the InP nanowires was carried out by scanning electron microscopy (SEM), high resolution transmission electron microscopy (HRTEM), and scanning transmission electron microscopy (STEM). An SEM image of a sample grown at a bias of 2 V is shown in Figure 3a. Nanowire growth is almost exclusively limited to a narrow region within 200−300 nm of the electrode edge, and bismuth islands showing no nanowire growth are clearly visible farther away from the electrode edge. The focusing of nanowire growth along the electrode edges correlates well with the magnitude of the electric field in the simulation shown in Figure 2e. As can be seen in the HRTEM image in Figure 3b, the nanowires tend to be polycrystalline, as could be expected from the frequent changes in wire-shape and direction seen in Figure 3a. This behavior could be related to the zinc-blende crystal structure of InP and the twinning behavior observed in MOCVD grown InP nanowires by Woo *et al.*[29] In contrast, CdSe nanowires grown by the EC-SLS technique show a high degree of crystallinity owing to their preferred growth direction along the (001) axis of the wurtzite crystal lattice.[13] We attribute the approximately 5 nm thick amorphous

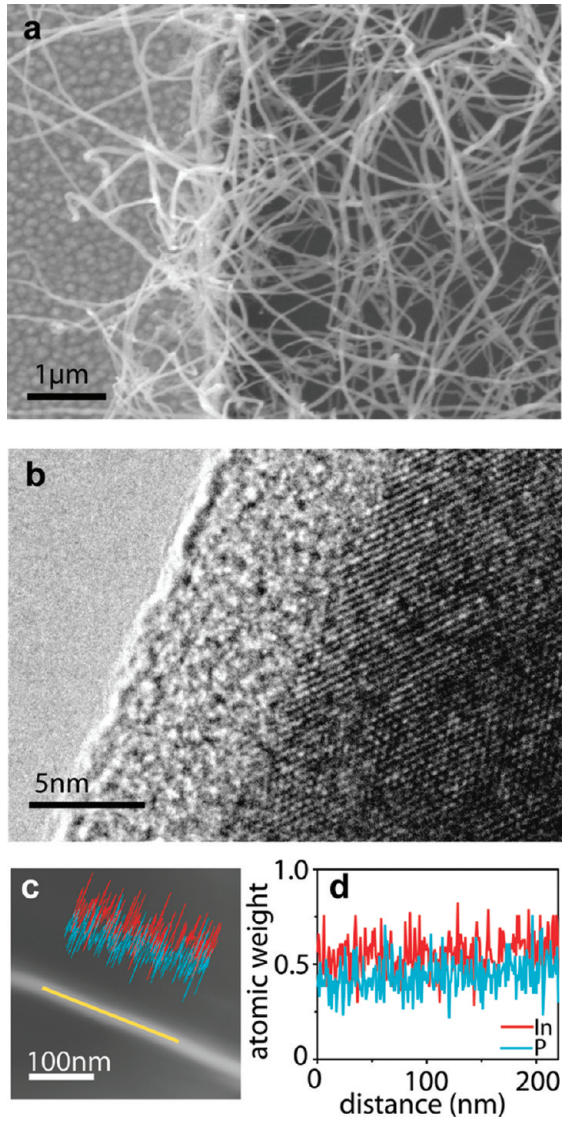


Figure 3. InP nanowire characterization. (a) Scanning electron microscope image of InP nanowires grown off the edge of a platinum electrode with bismuth beads on the surface; scale bar = 1 μm. (b) High resolution transmission electron microscope image of an InP nanowire; scale bar = 5 nm. (c) Scanning transmission electron microscope image of an InP nanowire used for elemental analysis; scale bar = 100 nm. (d) Relative atomic weight of indium and phosphorus as a function of position along the line highlighted in panel c, obtained from energy dispersive X-ray spectroscopy.

outer layer to the formation of a native oxide layer. Figure 3c highlights the line-scan along the wire used for elemental analysis by STEM shown in Figure 3d. The higher average atomic percentage of indium, 56%, relative to phosphorus, 44%, can be attributed to the indium-rich native oxide layer typically observed on InP.[30]

The current across three electrode pairs, connected in parallel, during the growth of InP nanowires at a constant bias of 1 V is plotted in Figure 4. The pure TOP solution is relatively insulating with a conductivity below 3 μS. Drop-wise injection of the indium and phosphorus precursors begins at 100 s and the growth-solution

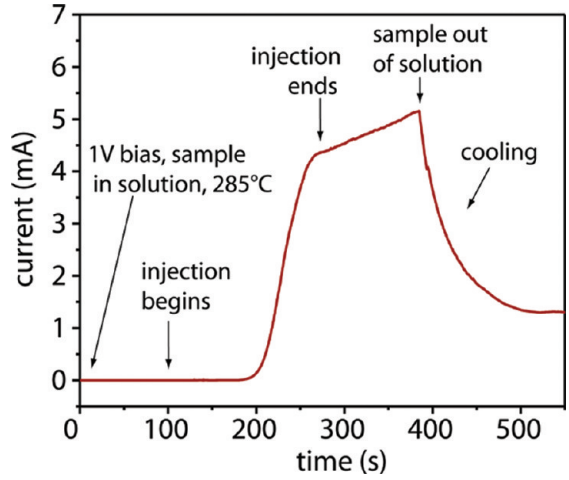


Figure 4. Current sensing across the electrode gap during the InP nanowire growth process as a function of time and at a constant bias of 1 V.

maintains its low initial conductivity until the current begins to rapidly increase at ~200 s. The rapid increase in current slows down at ~260 s and precursor injection is completed at 280 s. The current then shows a slow linear increase over the period from 280 to 400 s, while the sample remains in solution under constant bias. When the sample is withdrawn from the solution around 400 s the current shows a sharp decrease.

We interpret the rapid increase in current at ~200 s as the onset of InP nanowires bridging the electrode gap. If the increase in current were solely due to an increase in conductivity of the growth solution as the indium and phosphorus precursors are added, the current increase could be expected to set in immediately after precursor injection begins around 100 s. We also measured the conductivity of the indium and phosphorus precursors by only injecting one of the two precursors under otherwise identical synthesis conditions. In both cases the conductivity remained below 3 μS during the entire run, more than a factor of 1000 below the peak conductivity value in Figure 4. This indicates that the observed increase in current at ~200 s results from InP nanowires bridging the electrode gap. We interpret the nearly 100 s delay between the beginning of precursor injection and the rapid increase in current as the time it takes the InP nanowires to grow across the 10 μm wide electrode gap. The slow increase in current after precursor injection ends at 280 s could be due to additional bridging events resulting from wire growth from residual precursors in solution. However, chemical effects related to doping or better contact formation at the nanowire/electrode interface could also be responsible for the increase in current. The sharp decrease in current when the sample is withdrawn from the growth solution at 400 s can be attributed to a decrease in the number of thermally activated charge carriers as the sample cools (for a detailed discussion see Supporting Information). This suggests that monitoring the con-

ductivity during the EC-SLS growth process may serve as a useful tool for assessing *in situ* device formation.

The conductivity at 5 V of a series of devices grown at different bias voltages is plotted in Figure 5. The measurements were taken in a probe station under ambient conditions after removing the samples from solution and rinsing them with hexanes. When both electrodes were grounded during growth, only a small amount of wire growth resulting in a relatively low conductivity was observed. As in the case of CdSe, InP wire growth is inhibited at zero bias when the bismuth catalyst particles are in contact with the platinum electrodes up to temperatures exceeding 310 °C. In contrast, normal SLS nanowire growth is observed under otherwise identical growth conditions when the bismuth seed particles are placed on an insulating substrate like silicon oxide. Growth inhibition on platinum substrates is probably due to electron depletion of the bismuth particles resulting from the difference in work function between the two metals.[31] Applying a voltage reverses this effect on the low potential electrode by inducing a negative surface charge and hence compensating for electron depletion by the platinum substrate. The exact chemical reactions that take place when the indium and phosphorus in the precursor compounds are taken up by the bismuth catalyst seed particles are still unknown. Growth inhibition from electron depleted bismuth seed particles on platinum substrates could be related to a diminished ability of the bismuth to reduce and uptake indium. The small amount of InP nanowire growth, even at zero bias, could be related to the titanium adhesion layer that is exposed at the electrode edges or to bismuth particles that have migrated off the platinum electrodes onto the insulating substrate. When a growth bias of 0.5 V is applied, the average device conductivity increases by over an order of magnitude to about 2×10^{-5} S and a similar conductivity is observed for devices grown at 1 and 2 V. The saturation in conductivity as a function of growth voltages is surprising since there is a clear increase in wire material as a function of growth voltage as can be seen in Figure 2a−c. An explanation could be that the number of active catalyst seed particles at the electrode edges is similar for different growth voltages. The difference in overall wire material would then arise from an increase in wire length as a function of growth voltage, with a similar number of bridging nanowires largely independent of growth voltage. However, processes at the nanowire−electrode contacts and more complex electrochemical effects may also be involved. The inset in Figure 5 shows the *I*−*V* curves of three devices grown in parallel at 2 V. The conductivity suppression around zero bias is typical for Schottky

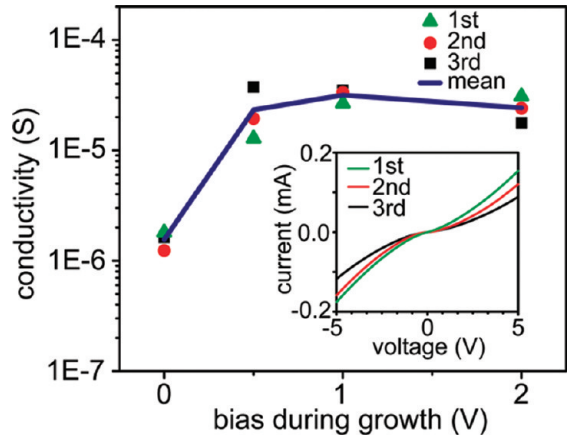


Figure 5. Conductivity as a function of bias voltage during growth. The conductivity, measured at a bias of 5 V, for three devices fabricated in parallel under the same conditions is plotted as a function of growth voltage. The inset shows the *I*−*V* curves of three devices grown in parallel at a bias of 2 V.

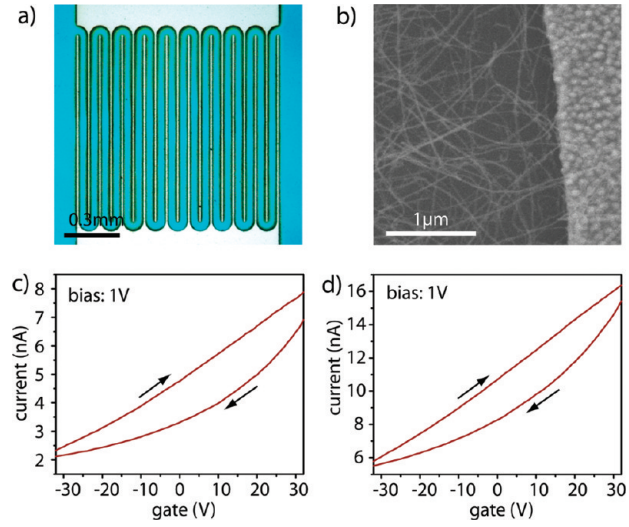


Figure 6. InP nanowire mats grown in a field effect transistor geometry. (a) Optical image of the InP nanowire field effect transistor device. (b) Scanning electron microscope image of a region of the device shown in panel a. (c and d) Current as a function of back gate voltage at a constant electrode bias of 1 V for two devices.

barrier formation in metal−semiconductor−metal contacts.

To determine the majority charge carrier type, we grew InP nanowire mats in a field effect transistor geometry using the EC-SLS technique (Figure 6a). Nanowire growth was carried out with one electrode grounded and the counter-electrode and doped silicon back gate held at +0.5 V in order to promote nanowire growth along the substrate surface. An SEM image of InP nanowires grown in transistor geometry is shown in Figure 6b. Current traces as a function of back gate voltage, at a constant bias of 1 V, are shown for two devices in Figure 6c,d. The observed hysteretic behavior may be related to trapping of charge carriers by the native oxide layer. The gating characteristics of both devices indicate that the ma-

jority of charge carriers in our EC-SLS grown InP nanowire mats are n-type.

CONCLUSION

We have demonstrated the electrically controlled solution−liquid−solid (EC-SLS) process for InP nanowires. A particularly attractive feature is our ability to monitor the bridging of nanowires across the electrode gap during the growth process, by simultaneously measuring the conductivity. Nanowire growth by the EC-SLS process has been shown to be a versatile and general process and could facilitate the direct integration of a wide variety of solution processed nanowires[32] and oriented nanowire heterostructures[26] into functional device geometries. The detailed processes underlying the EC-SLS process remain a point of scientific interest.

MATERIALS AND METHODS

The experimental setup is shown in Figure 1, additional details can be found in ref 13.

Sample Preparation. Interdigitated electrodes (5 nm titanium adhesion layer, 75 nm platinum layer, 20 nm bismuth catalyst layer, thermally evaporated) with a channel length of about 55 mm and a width of about 10 μm were defined on fused silica substrates (12.5 mm × 12.5 mm × 0.5 mm, MTI Corp.) by optical lithography. Samples used for the field effect transistor geometry consisted of interdigitated electrodes with a channel length of 18 mm and a width of 50 μm on degenerately doped silicon substrates with a 300 nm layer of insulating thermal oxide. As before, the electrodes consisted of a 5 nm Ti layer, a 75 nm Pt layer, and a 20 nm Bi layer.

Synthesis. A four-neck reaction flask was filled with 45 mL of tri-*n*-octylphosphine (Strem, 97%) under air-free conditions and heated to 285 °C. A stock solution of 0.25 M InI_3 (Alfa Aesar, 99.999%) in oleyl amine (Acros Organics, previously degassed under vacuum at 120 °C for 2 h) was prepared under nitrogen atmosphere. A 2 mL portion of the 0.25 M InI_3 stock solution was then added to 500 mg of tris(diethylamino)phosphine (Alfa Aesar). The resulting precursor solution was injected dropwise over the course of 3 min into the reaction flask containing the biased electrodes immersed in TOP at 285 °C.

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Supporting Information Available: Optical images of InP nanowire growth from the low potential electrode and additional SEM images of InP nanowires grown by EC-SLS. An analysis of the temperature dependence of InP nanowire conductivity as well as an example of InP SLS growth on an insulating substrate are provided. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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